TIGER YE

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SKILLS

Software: Verilog, System Verilog, C++, Python, Java, Git, MATLAB, C#, C, TCL

Other: UVM, Arduino, LT Spice, PCIe Spec, Vivado, Selenium, Microsoft Office, Confluence

WORK EXPERIENCE

Marvell Technology | Digital Design Verification — Jan 2024 - Aug 2024

- Improved and updated testbenches to better comply with **UVM** standards and changes in chip architecture
- Identified and resolved regression failures by analyzing **logfiles** and **waveform** data
- Completed **PCIe** MindShare course, gaining in-depth understanding of PCIe specification, specifically 6.0

Register Field Comparison Script

- Developed **Python** script to compare 3rd-party HTML registers with company files, identifying discrepancies
- Implemented capability walk functionality to identify and verify **PCIe capability structure** with expected

PCIe 6.0 L0p UVM Test Sequence

- Designed and tested **L0p UVM** sequence to verify entry into **L0p** for different lane widths and conditions
- Gained in-depth knowledge of **L0p** specifications and edge cases, which were each thoroughly covered
- Debugged testbench failures using transaction logfiles to determine if issue was **RTL** or **VIP** related

ArchES Computing | FPGA Design Engineer — May 2023 - Aug 2023

- Upgraded **FPGA** Test Platform to support multiple SFPs, send **IGMP** join requests, and respond to **ICMP** and **ARP**
- Migrated legacy platforms to new shell system, enabling uninterrupted operation while being reprogrammed
- Created **unit tests** for new and existing modules such as the width conversion, statistics, and network modules

AXI4-Stream Width Conversion Module

- Iterated through multiple width conversion algorithms to find the most resource efficient solution
- Analyzed synthesized **schematic** to identify and fix unintended areas of high resource usage resulting from **HLS**
- Developed an highly efficient width conversion module in **C++** using bit-shifting and template recursion

VN Instruments | R&D Associate — Sep 2022 - Dec 2022

- Designed a custom 80V power module **PCB** in **KiCAD** and fabricated an enclosure for it using **Fusion 360**
- Used **LT Spice** to model voltage regulators and debug issues involving start-up voltage
- Wrote **Python** and **TCL** scripts to generate pin settings based on csv files and automatically synthesize designs

Custom Communication Protocol for Data Synchronization

- Developed **Verilog** code for precise transfer of timestamp data between **FPGA**s using 3 signal lines
- Debugged data bus issues between **FPGA** and microcontroller communication using **oscilloscope** and **voltmeter**
- Wrote comprehensive **System Verilog** testbenches to ensure designs met functionality and timing requirements

PROJECTS

Ultrasonic Distance Measuring Tool — Nov 2022 - Dec 2022

- Designed a custom **PCB** to measure distances by sending ultrasonic pulses and measuring return time
- Researched and analysed part **datasheets** on Digikey to decide on components for **PCB**
- Wrote **Arduino** code for ATtiny85 microcontroller with **pin interrupts** to display distance on 14 segment display
- Iterated through multiple enclosure designs in **SOLIDWORKS** to create 3D printed snap fit shell for PCB

EDUCATION

University of Waterloo, Candidate for BASc, Mechatronics Engineering — Sep 2020 - Apr 2025